# NeoLoch

# Inquisitor 9060 DRAM Blade Manual

## Overview

The Inquisitor 9060 DRAM blade is designed to test 22 pin DRAM ICs. The Inquisitor 9060 DRAM tester can conduct fast two pass test or a more in depth test to discover if a DRAM is good or bad.

## August 2017

This document details the operation of the default configuration of the IC tester as well as details on the device's operation for custom code design.

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# 1.0 Device Connection & Power Requirements

## 1.1 CN1 – Card Edge Connector

Edge of PC board that plugs into the card edge socket on the Inquisitor Core PC board. When plugging in the SRAM Blade, line up the white triangle with the white triangle on the Core PC board.

## 1.2 CN2 – ICSP (In-Circuit Serial Programming)

ICSP connector, this port is designed to attach to a PICKit 3 or compatible programmer.

## 1.3 LED 1 – Power LED

Indicates when power is applied to the Blade.

## 1.4 Power Requirements

| | Minimum | Typical | Maximum |
|---|---|---|---|
| VCC | 4.5V | 5.0V | 5.5V |
| VDD | 10.8V | 12.0V | 13.2V |
| VBB | -4.5V | -5.0V | -5.5V |

Make sure the +12V side is using a regulated source. These DRAM ICs use the +12V supply as part of their power scheme. The -5V is supplied via the TC7662 voltage inverter and will be the opposite of the +5V supply.

# 2.0 Understanding the DRAM Testing Process

To begin testing a DRAM, use the following steps:

- Insert the DRAM blade into the Core module.
- Power up the tester.
- Insert the DRAM IC to be tested into the ZIF socket, make sure pin 1 is the closest pin to the ZIF's lever.
- Lower the lever to lock the DRAM in place.
- Press the left or right arrow key to select 9060 test.
- Press the enter key to start the test.

## 2.1 Menu System & DRAM Testing

Pressing the ← or → keys will guide your through the menu system, which consists of:

### 2.1.1 – 9060

Test 9060 DRAM and compatible DRAM select this menu item.

### 2.1.2 – Long Test

Determines if a long or short test is done when testing DRAM, yes = long test and no = short test.

**Short Test:** The DRAM is written with all zero's and then all one's. This is a quick test but may not discover all problems with a bad DRAM, this test consists of:
**Note:** as of firmware verions 2.1, the short test is no longer available on the 4027, 4096 and UPD414 tests.

Scan 1: Writes all zeroes to the DRAM and then reads the data back for comparison.
Scan 2: Writes all ones to the DRAM and then reads the data back for comparison.

**Long Test:** The long test does a far more extensive investigation of the DRAM and will discover problems the short test will miss. This test consists of:

Scan 1: Writes all zeroes to the DRAM and then reads the data back for comparison.

Scan 2: Writes all ones to the DRAM and then reads the data back for comparison.

Scan 3 – 18: The long test is a far more intensive look at the DRAM's capability to store, retain, and retrieve data correctly. The idea behind this test is to write a wide variety of changing data to each and every address. To accomplish this in a timely manner the following scheme is used:

First, the DRAM's memory is divided up into 8 bit chunks (bytes).

Two counters are used to generate values for the upper and lower nibbles. Counter 1 decrements and counter 2 increments. The low nibble of counter 1 is placed in the current DRAM's address range upper nibble, and the lower nibble of counter 2 is placed in the lower nibble. So:

DRAM bits 7 – 4 = Counter 1's lower four bits (lower nibble).
DRAM bits 3 – 0 = Counter 2's lower four bits (lower nibble).

So, if counter 1 & 2 both = 0 and we are on the very first byte range in the DRAM's memory, then bits 0 through 7 DRAM would all be clear. Byte 0 (address's 0 through 7) = 0x00.

Next, counter 1 is decremented, so would equal 0xFF. Counter 2 is incremented and equals 0x01. The following table illustrates this process and how the data changes for each byte in the DRAM over each scan.

| | Scan 3 | Scan 4 | Scan 5 | Scan 6 | Scan 7 | Scan 8 | Scan 9 | ... |
|---|---|---|---|---|---|---|---|---|
| Bits 0-7 (Byte 0) | 0xF1 | 0xE2 | 0xD3 | 0xC4 | 0xB5 | 0xA6 | 0x97 | ... |
| Bits 8-15 (Byte 1) | 0xE2 | 0xD3 | 0xC4 | 0xB5 | 0xA6 | 0x97 | 0x88 | ... |
| Bits 16-23 (Byte 2) | 0xD3 | 0xC4 | 0xB5 | 0xA6 | 0x97 | 0x88 | 0x79 | ... |
| Bits 24 -31 (Byte 3) | 0xC4 | 0xB5 | 0xA6 | 0x97 | 0x88 | 0x79 | 0x6A | ... |
| Bits 32 -39 (Byte 4) | 0xB5 | 0xA6 | 0x97 | 0x88 | 0x79 | 0x6A | 0x5B | ... |
| Bits 40 -47 (Byte 5) | 0xA6 | 0x97 | 0x88 | 0x79 | 0x6A | 0x5B | 0x4C | ... |
| Bits 48 -55 (Byte 6) | 0x97 | 0x88 | 0x79 | 0x6A | 0x5B | 0x4C | 0x3D | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... |

For 9060 DRAM the tests takes between 7 and 12 seconds, depending on the speed of the DRAM being tested.

### 2.1.2 – LED Color Setting

Changing this setting will reverse the LED colors, change this if you find the LED is turning red when an IC passes and green when it fails. This means the bi-color LED was installed backwards and changing this setting will correct that error.

### 2.1.4 – Statistics

To access statistics first press the left or right arrow key to clear the bad ram detect flag and then return to the test you wish to see statistics for. The press the down arrow key, statistics will be displayed which included the total number of tests, how many passed and how many failed. This menu item will only be displayed when the bad ram flag is clear.

### 2.1.5 – Multiple Scans Per Test

Changes the total number of tests conducted with a single press of the enter key. To access this feature first make sure the bad ram flag is clear, you can do this by pressing the left or right arrow key and then returning to the test you wish to modify. Next, press the down arrow key twice or the up arrow key once. You can change the setting using the following keys:

- Left Arrow: add 10 to the test total.
- Right Arrow: add 1 to the test total.
- Enter: Reset test total to 1.
- Up and Down: Move to next setting / return to test main menu.

Each test has it's own statistics and multiple scan setting.

Example: If you change the number of scans to 10 and then test a RAM, the test will be run 10 times on that RAM. This allows you to test a RAM multiple times without having to keep pressing the enter key for each test.

## 2.2 DRAM Speed Check

At the beginning of every test the MCU will attempt to determine the speed of the DRAM being tested. This speed test is done to get a general idea of how quickly the DRAM will respond to data requests and the internal testing process is adjusted to accommodate the DRAM. However, due to the slow speed of the MCU the DRAM speed can only be estimated. The ranges are:

| DRAM Speed Range | LCD Screen Displays (top line, right side) |
|---|---|
| <= 218ns | “218” |
| 218ns to 686ns | “687” |
| 686ns to 1.2µs | “1.2” |
| 1.2µs to 1.6µs | “1.6” |
| 1.6µs to 2.2µs | “2.2” |
| 2.2µs to 2.6µs | “2.6” |
| 2.6µs to 3.0µs | “3.0” |
| 3.0µs to 3.4µs | “3.4” |
| > 3.4 | “---” |

Seeing “---” displayed on the LCD screen mean the speed check failed, but does not mean the DRAM being tested is bad. Repeating the test will usually return a valid speed test value.

## 2.3 LED Result

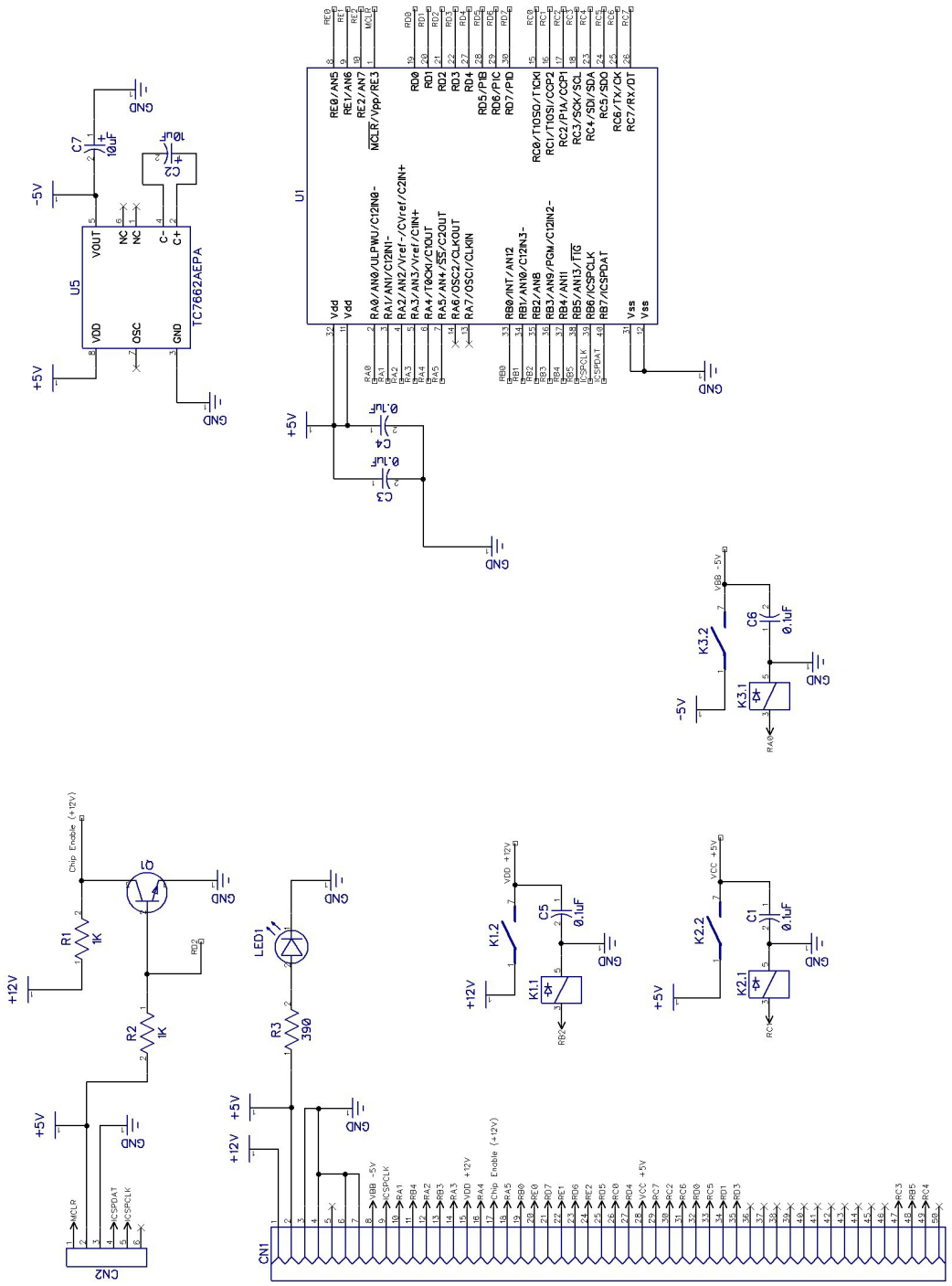
At the conclusion of a test, LED 3 on the main board will visually display the result. Green means the DRAM passed and red means the DRAM failed. During the test the LED will be orange.

## 2.4 Display DRAM Results.

If a DRAM tests bad, you can use the up and down arrows keys to get a better idea of what happened during each scan. The first address a bad bit was detected at is listed along with the number of bad bits encountered during that pass.

# 3.0 Schematic



# 4.0 Card Edge to MCU Connections

Below is a table that lays out the pin assignment between the card edge connector, the MCU and the Port Expander.

| Card Pin # | Function | Card Pin # | Function |
|---|---|---|---|
| 2 | +5V | 1 | +12V |
| 4 | Ground | 3 | Ground |
| 6 | Card Error LED (Gnd to turn LED off) | 5 | Not Connected |
| 8 | ZIF Pin 1 – VBB -5V | 7 | ZIF Pin 40 – GND |
| 10 | ZIF Pin 2 – MCU RA1 | 9 | ZIF Pin 39 – MCU RB6 (PGC) |
| 12 | ZIF Pin 3 – MCU RA2 | 11 | ZIF Pin 38 – MCU RB4 |
| 14 | ZIF Pin 4 – MCU RA3 | 13 | ZIF Pin 37 – MCU RB3 |
| 16 | ZIF Pin 5 – MCU RA4 | 15 | ZIF Pin 36 – MCU RA6 |
| 18 | ZIF Pin 6 – MCU RA5 | 17 | ZIF Pin 35 – MCU RB1 |
| 20 | ZIF Pin 7 – MCU RA7 | 19 | ZIF Pin 34 – MCU RB0 |
| 22 | ZIF Pin 8 – VDD +12V | 21 | ZIF Pin 33 – VCC +5V |
| 24 | ZIF Pin 9 – NC | 23 | ZIF Pin 32 – NC |
| 26 | ZIF Pin 10 – NC | 25 | ZIF Pin 31 – NC |
| 28 | ZIF Pin 11 – NC | 27 | ZIF Pin 30 – NC |
| 30 | ZIF Pin 12 – NC | 29 | ZIF Pin 29 – NC |
| 32 | ZIF Pin 13 – NC | 31 | ZIF Pin 28 – NC |
| 34 | ZIF Pin 14 – NC | 33 | ZIF Pin 27 – NC |
| 36 | ZIF Pin 15 – NC | 35 | ZIF Pin 26 – NC |
| 38 | ZIF Pin 16 – NC | 37 | ZIF Pin 25 – NC |
| 40 | ZIF Pin 17 – NC | 39 | ZIF Pin 24 – NC |
| 42 | ZIF Pin 18 – NC | 41 | ZIF Pin 23 – NC |
| 44 | ZIF Pin 19 – NC | 43 | ZIF Pin 22 – NC |
| 46 | ZIF Pin 20 – NC | 45 | ZIF Pin 21 – NC |
| 48 | Switches – MCU RB5 | 47 | I2C – SCL – MCU RC3 |
| 50 | Not Connected | 49 | I2C - SDA – MCU RC4 |

# 5.0 Parts List

- 1 – Printed circuit board
- 1 – 40 pin socket
- 1 – 8 pin socket
- 1 – PIC16F1719 microcontroller (Programmed)
- 1 – TC7662 Voltage Inverter.
- 3 – Reed Relays (Polarized)
- 1 – 390 Ohm Resistor (Orange, White, Brown)
- 1 – 2x5 rectangle green LED
- 5 – 0.1uF Ceramic Capacitors
- 2 – 10uF capacitor
- 2 – 1K Ohm Resistor (Brown, Black, Red)
- 1 – 4401 NPN Transistor.

# 6.0 Firmware Versions and Known Bugs

No known issues discovered at this time.

## 6.1 V1.0 MCU Firmware

Initial release of this product.

# 7.0 Cross Reference Chart

The following cross reference chart is intended to help guide you in determining if a specific DRAM may be testable using the 9060 blade. NeoLoch has not tested all the listed RAM and certainly not all the variants for each part number, and makes no guarantee that all variants are testable.

| Manufacturer | Test | Notes: |
|---|---|---|
| AMD | AM9060 | |
| FAIRCHILD | | |
| FUJITSU | | |
| MOSTEK | | |
| MOTOROLA | MCM6605 | |
| NEC | UPD410<br>UPD411 | |
| NSC | MM4280<br>MM5280<br>MM5281 | |
| OKI | | |
| SIGNETICS | 2660<br>2680 | |
| TI | TMS4030<br>TMS4060 | |
| TOSHIBA | | |

# Appendix A: Firmware Revision History

**Firmware Version 1.0**

- Initial Release

# Appendix B: Document Revision History

**Revision A (8/2017)**

- Initial release of this document